

REMARKS

Claims 1-41 are pending. Reconsideration and allowance are respectfully requested.

Restriction

Claims 1-41 stand restricted under 35 U.S.C. §121, and the Examiner identified two (2) groups of claims: Group I (Claims 1-20) and Group II (Claims 23-41). It should also be noted that the Examiner failed to address Claims 21 and 22, but Applicant presumes that Claims 21 and 22 belong to Group I. Applicant respectfully traverses this restriction; however, Applicant conditionally elects the Claims 23-41 of Group II to prosecute in the present application as required by the Examiner.

According to MPEP §808, the Examiner must show that (1) the inventions are distinct and (2) there would be a serious burden on the Examiner if restriction is not imposed. Applicant respectfully asserts that examination of all of the identified groups would not constitute a serious burden. MPEP §808.02 establishes the guidelines for determining a “serious burden,” which is as follows:

Thus the examiner must show by appropriate explanation one of the following:

(A) Separate classification thereof: This shows that each invention has attained recognition in the art as a separate subject for inventive effort, and also a separate field of search. Patents need not be cited to show separate classification.

(B) A separate status in the art when they are classifiable together: Even though they are classified together, each invention can be shown to have formed a separate subject for inventive effort when the examiner can show a recognition of separate inventive effort by inventors. Separate status in the art may be shown by citing patents which are evidence of such separate status, and also of a separate field of search.

(C) A different field of search: Where it is necessary to search for one of the inventions in a manner that is not likely to result in finding art pertinent to the other invention(s) (e.g., searching different classes/subclasses or electronic resources, or employing different search queries, a different field of search is shown, even though the two are classified together. The indicated different field of search must in fact be pertinent to the type of subject matter covered by the claims. Patents need not be cited to show different fields of search.

With respect to item A, separate classification is irrelevant. Regardless of whether these groups can be classified in different groups, a search of the relevant art of the independent claims art would necessarily yield art in the various classifications. It is well-known that Examiners do not perform searches for art in “shoes,” where classification was extremely important, as was the practice before the advent of computers and automated databases. In fact, Examiners conduct word searches on computer databases for patent and non-patent literature references, almost without regard for classification. Based on these word searches of the independent claims, it is clear that art relevant to each group would be yielded. Thus, no “serious burden” can be established for these closely related groups simply because they can be classified in different classifications.

With respect to item B, there is no separate status in the art because a search of the claims of Group II would yield prior art for Group I. Looking to Claims 1 (for example), which Applicant believes to be the broadest claim and which belongs to Group I, all of the limitations of Claims 1 are included (verbatim) in Claim 28. For the Examiner, convenience, a comparison between the limitations of Claims 1 and 28 is provided below, with the similar or the same limitation underlined.

Claim 1	Claim 28
A first-in-first-out memory, comprising:	A network node for controlling the transmission and receipt of packet-based data over a communications facility, comprising:
	a system interface for receiving transmit data from a system and for outputting processed received signals to the system;
	a transmit FIFO buffer, for buffering transmit data received at the system interface;
	a transceiver, for driving the communications facility with transmitted signals corresponding to the transmit data, and for receiving signals from the communications facility;
	a receive FIFO buffer, for buffering the received signals; and wherein each of the transmit and receive FIFO buffers comprise:
<u>a memory array;</u>	<u>a memory array;</u>
<u>a clock terminal for receiving a clock signal;</u>	<u>a clock terminal for receiving a clock signal;</u>
<u>a write enable terminal for receiving a write enable signal;</u>	<u>a write enable terminal for receiving a write enable signal;</u>
<u>inputs for receiving input data words;</u>	<u>inputs for receiving input data words;</u>
<u>a read enable terminal for receiving a read enable signal;</u>	<u>a read enable terminal for receiving a read enable signal;</u>
<u>outputs for presenting output data words of the same word width as that of the input data words;</u>	<u>outputs for presenting output data words of the same word width as that of the input data words;</u>
<u>a write buffer, coupled to the inputs and to the array of memory cells, for receiving a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal, and for writing the first and second input data words to the memory array in a single write cycle;</u>	<u>a write buffer, coupled to the inputs and to the array of memory cells, for receiving a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal, and for writing the first and second input data words to the memory array in a single write cycle;</u>
<u>read circuitry, for requesting a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and</u>	<u>read circuitry, for requesting a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and</u>
<u>a read buffer, for receiving first and second output data words from the memory array responsive to the request of the read of the memory array, and for presenting the first and second output data words in sequence to the outputs.</u>	<u>a read buffer, for receiving first and second output data words from the memory array responsive to the request of the read of the memory array, and for presenting the first and second output data words in sequence to the outputs.</u>

This same type of comparison can be made between Claim 16 (of Group I) and Claim 23 (of Group II). As a result, it is abundantly clear that searches related claims of Group II would result in the same or nearly the same prior art. Therefore, there is clearly no separate status in the art.

With respect to item C, a separate field of search is not required. The same arguments that apply to item A above apply to item C with equal force. Thus, no “serious burden” can be established for these closely related inventions because no separate field of search is required.

Accordingly, Applicant respectfully requests that the restriction requirement be withdrawn.

Conclusion

Applicant respectfully requests full allowance of Claims 1-41.

Applicant does not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account 20-0668 of Texas Instruments Incorporated.

Should the Examiner require any further clarification to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

/John J. Patti/

Dated: August 20, 2010

John J. Patti
Reg. No. 57,191
Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, Texas 75265
Phone: (972)917-4144